UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,362	04/12/2004	Fuk Ho Pius Ng	M102.12-0005	3073

27367 7590 08/13/2007

WESTMAN CHAMPLIN & KELLY, P.A.
SUITE 1400
900 SECOND AVENUE SOUTH
MINNEAPOLIS, MN 55402-3319

EXAMINER	
DO, CHAT C	
ART UNIT	**PAPER NUMBER**
2193	

MAIL DATE	DELIVERY MODE
08/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/822,362	PIUS NG ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/13/05;9/07/04;7/15/04;5/28/04;4/12/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 September 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09/07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-29 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 1-29 cite a method and circuit of adding a plurality of partial products in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application or a concrete, useful, and tangible result. However, claims 1-29 merely disclose steps/components for adding a plurality of partial products without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the idea embodied therein. Therefore, claims 1-29 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-29 are rejected under 35 U.S.C. 102(b) as being anticipated by Ichikawa (U.S. 5,978,827).

Re claim 1, Ichikawa discloses in Figures 1-40 a method of adding a plurality of partial products (e.g. abstract, and Figure 6 wherein the XxYxs are the partial products), wherein each partial product has a plurality of bits having respective binary weights (e.g. weights are cited in the first row in Figure 6), wherein each bit can have a first or second logic state (e.g. as either 0/1 in binary system), the method comprising: forming a first set of multiple-bit columns from bits of the plurality of partial products, wherein the bits in each column of the first set have the same binary weight (e.g. circle the column in the partial product section in Figure 6); and encoding each multiple-bit column in the first set into a respective modified partial product, which represents a number of bits in the column having the first logic state (e.g. by first addition of the column to yield respective sum of the column in the first addition section in Figure 6).

Re claim 2, Ichikawa further discloses in Figures 1-40 forming a second set of multiple-bit columns from bits of the modified partial products, wherein the bits bit in each column of the second set have the same binary weight as one another (e.g. repeating the same process as seen above for the column of result of first addition section as seen in Figure 22); and encoding each column in the second set into a respective further modified partial product, which represents a number of bits in the column having the first logic

state (e.g. by last addition of the column to yield respective sum of the column in the first addition section in Figure 22).

Re claim 3, Ichikawa further discloses in Figures 1-40 repeating the steps of forming and encoding to form successive sets of further modified partial products until the number of further modified partial products is reduced to a desired number (e.g. Figure 22 wherein repeating the above process until to yield three numbers as seen in second addition in Figure 22).

Re claim 4, Ichikawa further discloses in Figures 1-40 adding the desired number of further modified partial products to produce a product (e.g. the Qx as result of addition of the last stage of modified partial products in Figure 22).

Re claim 5, Ichikawa further discloses in Figures 1-40 for each multiple-bit column in the first set, forming a modified column word by packing all the bits in that column having the first logic state into a first contiguous set of bit positions in the modified column word (e.g. circle of column partial product in the partial product section in Figure 6); and generating the respective modified partial product based on a pattern of the first and second logic states in the modified column word (e.g. for instant the S32, S31, and S30 are the result of column of partial products of weight 2^3 as seen in Figure 6).

Re claim 6, Ichikawa further discloses in Figures 1-40 forming a modified column word comprises packing all the bits in that column having the first logic state to one end of the modified column word; and generating comprises generating the respective modified partial product based on the bit positions in the modified column word at which

values of the bits in the modified column word transition between the first and second logic states (e.g. repeating the whole process until to yield the last three modified partial products as seen in Figure 22).

Re claim 7, Ichikawa further discloses in Figures 1-40 the modified column word comprises first and second opposite ends and the step of forming the modified column word comprises, for each multiple-bit column in the first set: (a) grouping adjacent ones of the bits of the multiple-bit column into a present level of multiple-bit groups (e.g. by circling the column in Figure 6); (b) for each group in the present level, packing any of the bits in that group having the first logic state toward a first end of that group, which corresponds in orientation to the first end of the modified column word, to form a respective modified present level group (e.g. as the sum of high logic only in that column of partial product by counting the high logic level); (c) grouping adjacent ones of the modified present level groups into respective higher level groups, with the higher level groups becoming the present level groups (e.g. as the next column of partial product); (d) repeating step (b) for the present level groups generated in step (c) (e.g. repeat for the whole partial products in Figures 6 and 22); and (e) repeating steps (b) through (d) until there is only one present level group, which has the same number of bit positions as the modified column word and any of the bits in that group having the first logic state have been packed toward the first end of that group (e.g. Figures 6 and 22).

Re claim 8, Ichikawa further discloses in Figures 1-40 shifting the bits in that group having the first logic state to different bit positions in that group through a multiplexer (e.g. S22, S21, and S20 in Figure 4).

Re claim 9, it is a method having similar limitations cited in claim 1. Thus, claim 9 is also rejected under the same rationale as cited in the rejection of rejected claim 1.

Re claim 10, it is a method having similar limitations cited in claim 2. Thus, claim 10 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 11, it is a method having similar limitations cited in claim 3. Thus, claim 11 is also rejected under the same rationale as cited in the rejection of rejected claim 3.

Re claim 12, it is a method having similar limitations cited in claim 4. Thus, claim 12 is also rejected under the same rationale as cited in the rejection of rejected claim 4.

Re claim 13, it is a method having similar limitations cited in claim 5. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 5.

Re claim 14, it is a method having similar limitations cited in claim 6. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 15, it is a method having similar limitations cited in claim 7. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 16, it is a method having similar limitations cited in claim 8. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 8.

Re claim 17, Ichikawa further discloses in Figures 1-40 generating a plurality of partial products comprises, for each partial product: multiplexing the multiplicand multiplied by zero, the multiplicand multiplied by one, the multiplicand multiplied by minus one, the multiplicand multiplied by two, and the multiplicand multiplied by minus two to produce the respective partial product (e.g. as a Booth encoder in col. 3 lines 11-22).

Re claim 18, it is a circuit having similar limitations cited in claim 9. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 19, it is a circuit having similar limitations cited in claim 17. Thus, claim 19 is also rejected under the same rationale as cited in the rejection of rejected claim 17.

Re claim 20, it is a circuit having similar limitations cited in claim 10. Thus, claim 20 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 21, it is a circuit having similar limitations cited in claim 11. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 22, it is a circuit having similar limitations cited in claim 13. Thus, claim 22 is also rejected under the same rationale as cited in the rejection of rejected claim 13.

Re claim 23, it is a circuit having similar limitations cited in claim 14. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 14.

Re claim 24, Ichikawa further discloses in Figures 1-40 receiving an accumulation feedback value and using the accumulation feedback value as an additional member of the plurality of partial products in the steps of forming and encoding (e.g. accumulator in Figure 37).

Re claim 25, Ichikawa further discloses in Figures 1-40 the step of receiving an accumulation feedback value comprises receiving a plurality of feedback values and using the plurality of feedback values as additional members of the plurality of partial products in the steps of forming and encoding (e.g. accumulator in Figure 37).

Re claim 26, it is a method having similar limitations cited in claim 24. Thus, claim 26 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 27, it is a method having similar limitations cited in claim 25. Thus, claim 27 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Re claim 28, it is a circuit having similar limitations cited in claim 24. Thus, claim 28 is also rejected under the same rationale as cited in the rejection of rejected claim 24.

Re claim 29, it is a circuit having similar limitations cited in claim 25. Thus, claim 29 is also rejected under the same rationale as cited in the rejection of rejected claim 25.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 4,598,382 to Sato discloses a multiplying circuit.

b. U.S. Patent No. 6,708,193 to Zeng discloses a liner summation multiplier array implementation for both signed and unsigned multiplication.

c. U.S. Patent No. 4,495,593 to Ware discloses a multiple bit encoding technique for combinational multipliers.

d. U.S. Patent No. 5,796,645 to Peh et al. disclose a multiply accumulate computation unit.

e. U.S. Patent No. 4,884,233 to Ishizuka et al. disclose a fast summing circuit.

f. U.S. Patent No. 6,742,174 to Chen et al. disclose a similarity-driven synthesis for equivalence checking of complex designs.

g. U.S. Patent No. 6,029,187 to Verbauwhede discloses a fast regular multiplier architecture.

h. U.S. Patent No. 6,535,901 to Grisamore discloses a method and apparatus for generating a fast multiply accumulator.

i. U.S. Patent No. 7,139,788 to Talwar et al. disclose a multiplication logic circuit.

j. U.S. Patent No. 5,978,827 to Ichikawa discloses an arithmetic processing.

k. U.S. Patent No. 2004/0128336 to Zierhofer discloses a method and system for multiplication of binary numbers.

l. U.S. Patent No. 2004/0139138 to Chen et al. disclose a method and apparatus for efficient bi-linear interpolation and motion compensation.

m. U.S. Patent No. 2003/0101207 to Dhong et al. disclose a random carry-in for floating-point operations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

August 8, 2007